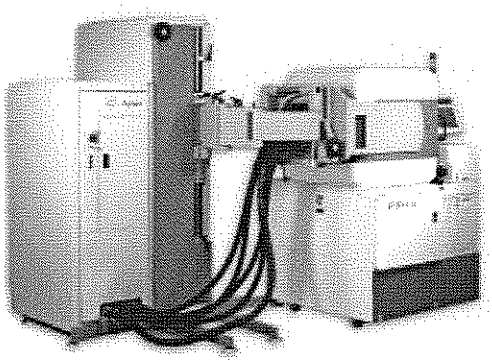
EXHIBIT RR

Evaluation Engineering

Making Fewer Touchdowns Saves Time

by Tom Lecklider, Technical Editor



Cost of test (CoT) is the single number that determines a semiconductor manufacturer's level of flash memory test success. Achieving a truly low CoT results from adopting multisite probing during at-speed wafer testing, making profitable use of the floor space a smaller machine occupies, and increasing throughput by using a tester-per-site ATE architecture. But reliability, flexibility, and ease of programming also are important factors.

The new Versatest Series V4400 Flash Memory Test System from Agilent Technologies addresses all these issues and more. Third-generation water-cooling supports circuit packaging so dense that all the electronics required for 36 test sites are mounted in the test head. Custom CMOS ASICs and micro-via PCBs integrate Tester-Per-Site™ architecture having 64 pins in a single-site module. Nine of these modules, a clock board, and five power supplies comprise a quadrant within the test head.

On a per-quadrant basis, eight single-site modules can be combined to create a 512-channel super site. Because each 64-pin site can be subdivided into four 16-pin groups and NAND devices have only 16 pins, this is one approach to ×32 NAND device probing. In this case, the small pin-count of the device is taken into account to minimize the tester hardware required. Alternatively, a single large device might require super-site treatment.

As the term quadrant implies, these examples use a fourth of the possible 2,304 pins. The overall 36-site capability provides four more sites than a conventional ×32 configuration. Consequently, 36-site parallel probing generates a 12% throughput improvement,

even allowing for the statistically longer test time one of the additional four devices may require. Having nine possible multisite probe layouts to choose from rather than six in a ×32 system also ensures probe-pattern efficiency.

The pins are fast and accurate. The basic clock speed of 100 MHz can be doubled to 200 MHz in the shared resourceMUX mode, supporting a 100-MHz data rate. Overall timing accuracy is ±1.0 ns, and all pin timing, period, and format settings are made on the fly. Clocking at 40, 70, or 100 MHz for flash, burst-mode, or embedded-memory devices is only part of the V4400's flexibility.

Patterns, Patterns, Patterns

The heart of each tester module is the algorithmic pattern generator (APG) and its sequencer that can address up to 16-Mwords of microprocessor memory. That's a large memory, but even the standard 4-Mword memory can be extended by the basic continue, jump, call, return, repeat, and next instruction set. For example, the same microinstruction can be repeated up to 64k times, and there is a 16-deep stack for nested subroutines.

Three 16-bit address generators, two data generators, and three counters form part of the APG resources, each with a uniform instruction set. The period generator has a range of 15 ns to 300 μs with 5-ns resolution and a fine period resolution of 312.5 ps. This generator provides system pipeline clocks and pattern startup and shutdown.

Rounding out the APG are the I/O access control, data multiplexing, and pipeline registers for specific control bits. The I/O access section produces pattern-generator I/O signals and supports pointer auto-increment functions for write and read operations. The data multiplexing circuitry contains multiplexers for buffer memory or data-generator source selection and address/data selection.

A split-ground design ensures the DUT measurements won't be affected by high-speed digital switching. In addition, reliability has been enhanced through ASIC integration and by eliminating all mechanical relays from the pin electronics modules.

The test-head effectively is the complete 36-site test system. The only connections to it are water hoses, DC power, and fiber-optic communications lines from the controlling PC. Delivery of the V4400 is Q1, 2001. Starts at $560,000. **Agilent Technologies**, 800-452-4844.